OLED Module

P27701

This data sheet was provided by

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Preliminary Specification

PRODUCT NAME: RGS24128064YR000
PRODUCT NO.: 9OL9927701000

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2013. 01. 18	

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : Yellow
- Panel resolution : 128*64
- Driver IC : SPD0301
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 2.027 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8-bit 6800/8080-series parallel interface, Serial Peripheral Interface, I^2C Interface.
- Wide range of operating temperature : -40 to 70℃
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 x 64	dot
2	Dot Size	0.4 (W) x 0.4 (H)	mm^2
3	Dot Pitch	0.43 (W) x 0.43 (H)	mm^2
4	Aperture Rate	86	%
5	Active Area	55.01 (W) x 27.49 (H)	mm^2
6	Panel Size	60.5 (W) x 37 (H)	mm^2
7	Panel Thickness	1.82 ± 0.1	mm
8	Module Size	60.5 (W) x 47 (H) x 2.027 (T)	mm^3
9	Diagonal A/A size	2.4	inch
10	Module Weight	TBD	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	4	V	Ta = 25℃	IC maximum rating
Supply Voltage (Vcc)	8	17	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	70	℃		
Storage Temp	-40	85	℃		
Humidity	-	85	%		
Life Time	40,000	-	Hrs	90 cd/m^2, 50% checkerboard	Note (1)
Life Time	50,000	-	Hrs	70 cd/m^2, 50% checkerboard	Note (2)
Life Time	70,000	-	Hrs	50 cd/m^2, 50% checkerboard	Note (3)

Note:

(A) Under Vcc = 14V

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 90 cd/m^2 :

- Contrast setting : 0xaf
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 70 cd/m^2 :

- Contrast setting : 0x6f
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 50 cd/m^2 :

- Contrast setting : 0x3f
- Frame rate : 105Hz
- Duty setting : 1/64

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Operating Voltage	-	13.5	14	14.5	V
V_{DD}	Logic Supply Voltage	-	1.65	-	3.3	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9* V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8* V_{DD}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2*V_{DD}	V
$I_{DD, SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~16V Display OFF, No panel attached	-	-	10	uA
$I_{CC, SLEEP}$	Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~16V Display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} =12, IREF =10uA, No Panel attached, Display ON, All ON	Contrast = FFh	-	450	580	uA
I_{DD}	V_{DD} Supply Current V_{DD} =2.8V, V_{CC} = 12, IREF = 10uA , No Panel attached, Display ON, All ON,		-	90	110	uA
I_{SEG}	Segment Output Current, V_{DD} = 2.8V, V_{CC} =12V, IREF=10uA, Display ON.	Contrast=FFh	280	310	340	uA
		Contrast=AFh	-	215	-	
		Contrast=7Fh	-	155	-	
		Contrast=3Fh	-	78	-	
		Contrast=0Fh	-	20	-	

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption	-	28.5	30.5	mA	All pixels on
Standby mode current consumption	-	3	5	mA	Standby mode 10% pixels on
Normal mode power consumption	-	399	427	mW	All pixels on
Standby mode power consumption	-	42	70	mW	Standby mode 10% pixels on
Pixel Luminance	50	70		cd/m^2	Display Average
Standby Luminance		35		cd/m^2	
CIEx (Yellow)	0.43	0.47	0.51		CIE1931
CIEy (Yellow)	0.45	0.49	0.53		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

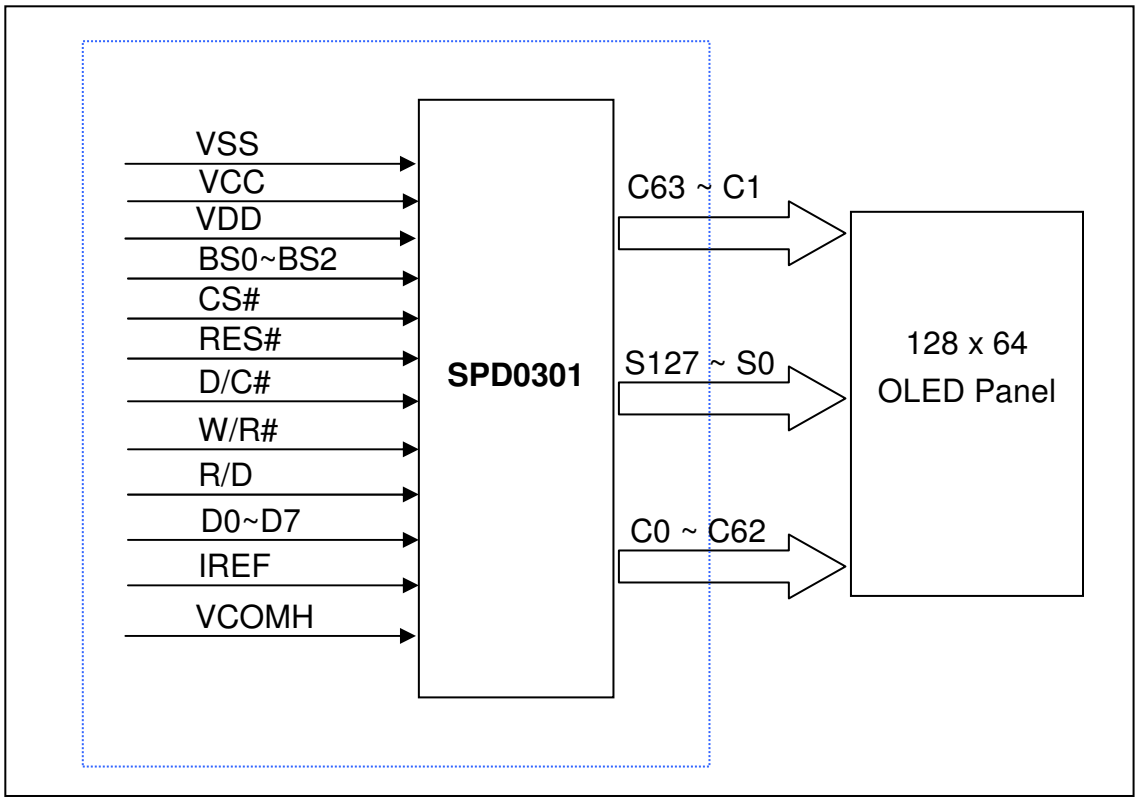
- Driving Voltage : 14V
- Contrast setting : 0x6f
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Standby mode condition :

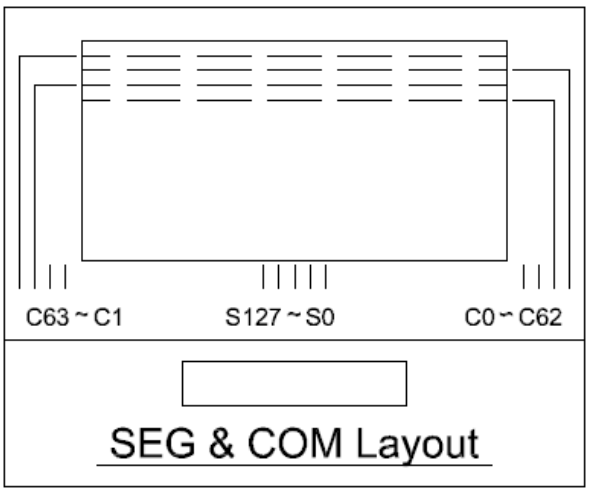
- Driving Voltage : 14V
- Contrast setting : 0x0a
- Frame rate : 105Hz
- Duty setting : 1/64

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
VSS	1	Ground pin.
VCC	2	Power supply for panel driving voltage.
VDD	3	Power supply pin for core logic operation.
BS0	4	MCU bus interface selection pins.
BS1	5	
BS2	6	
CS#	7	This pin is the chip select input connecting to the MCU.
RES#	8	This pin is reset signal input.
D/C#	9	This pin is Data/Command control pin connecting to the MCU.
W/R#	10	This pin is read / write control input pin connecting to the MCU interface.
R/D	11	This pin is MCU interface input.
D0	12	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
D1	13	
D2	14	
D3	15	
D4	16	
D5	17	
D6	18	
D7	19	
IREF	20	This pin is the segment output current reference pin.
VCOMH	21	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.
VCC	22	Power supply for panel driving voltage.
VSS	23	Ground pin.

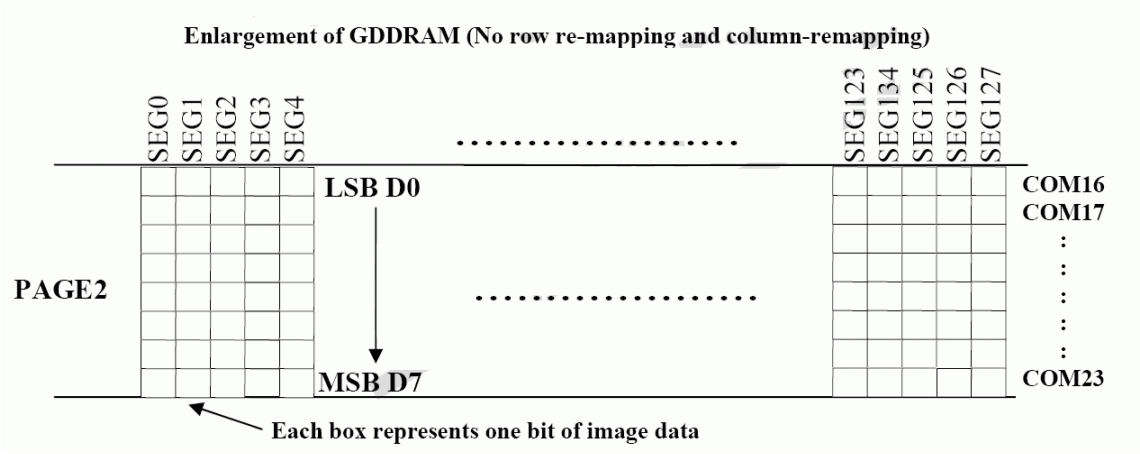
7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in below figures.

GDDRAM pages structure of SPD0301

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM 63-COM56)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM 55-COM48)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM47-COM40)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM39-COM32)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM31-COM24)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM23-COM16)
PAGE6 (COM48–COM55)	Page 6	PAGE6 (COM15-COM8)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM 7-COM0)
	SEG0 ----------SEG127	
Column re-mapping	SEG127 ----------SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in below figures.



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

7.5 INTERFACE TIMING CHART

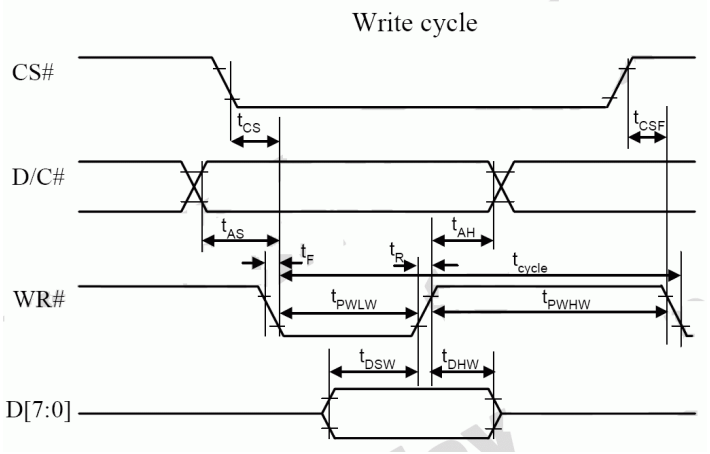
8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V ~3.3V, T_A = 25°C)

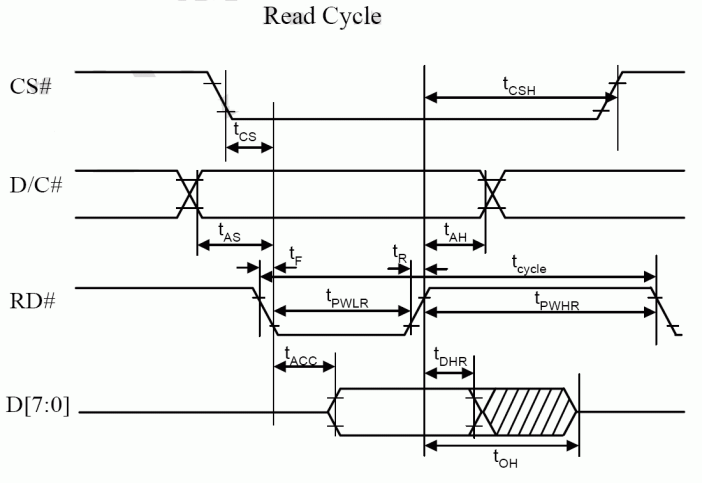
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics

Write cycle



Read Cycle



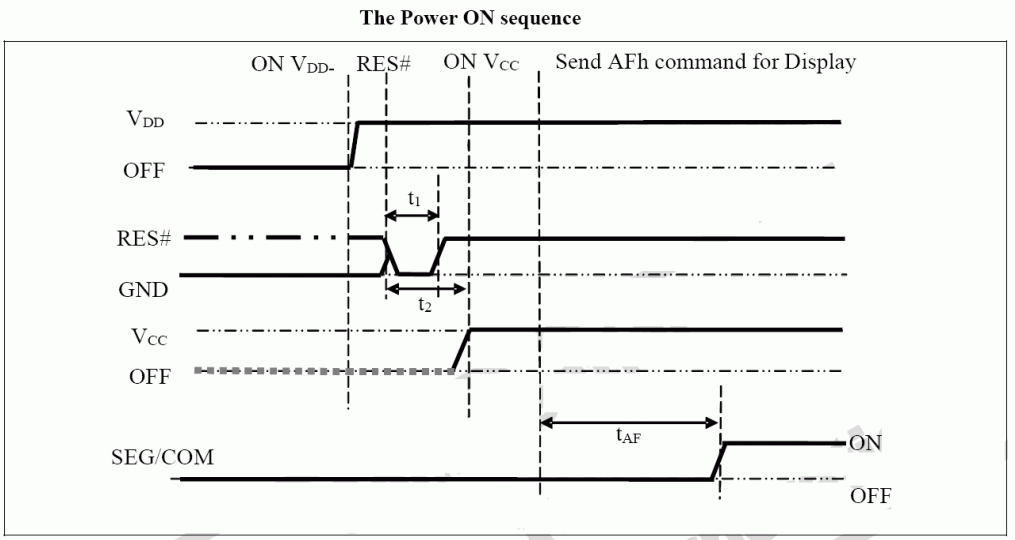
8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SPD0301

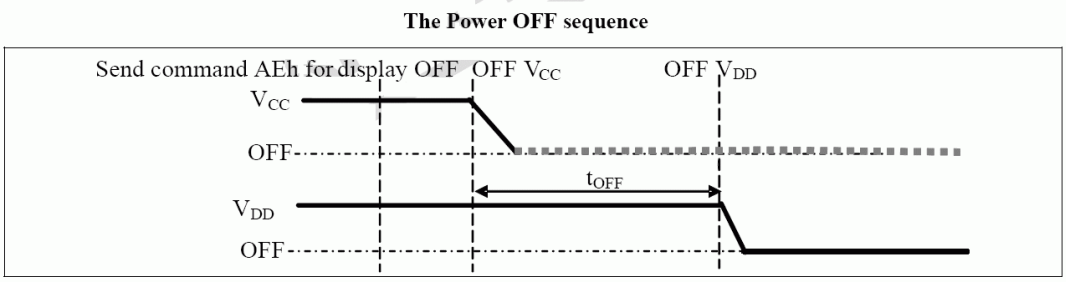
***Power ON sequence*:**

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [3] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. [1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).



***Power OFF sequence*:**

1. Send command AEh for display OFF.
2. Power OFF V_{CC} [1], [2]
3. Power OFF V_{DD} after t_{OFF}.[4] (where Minimum t_{OFF}=80ms,Typical t_{OFF}=100ms)



Note:

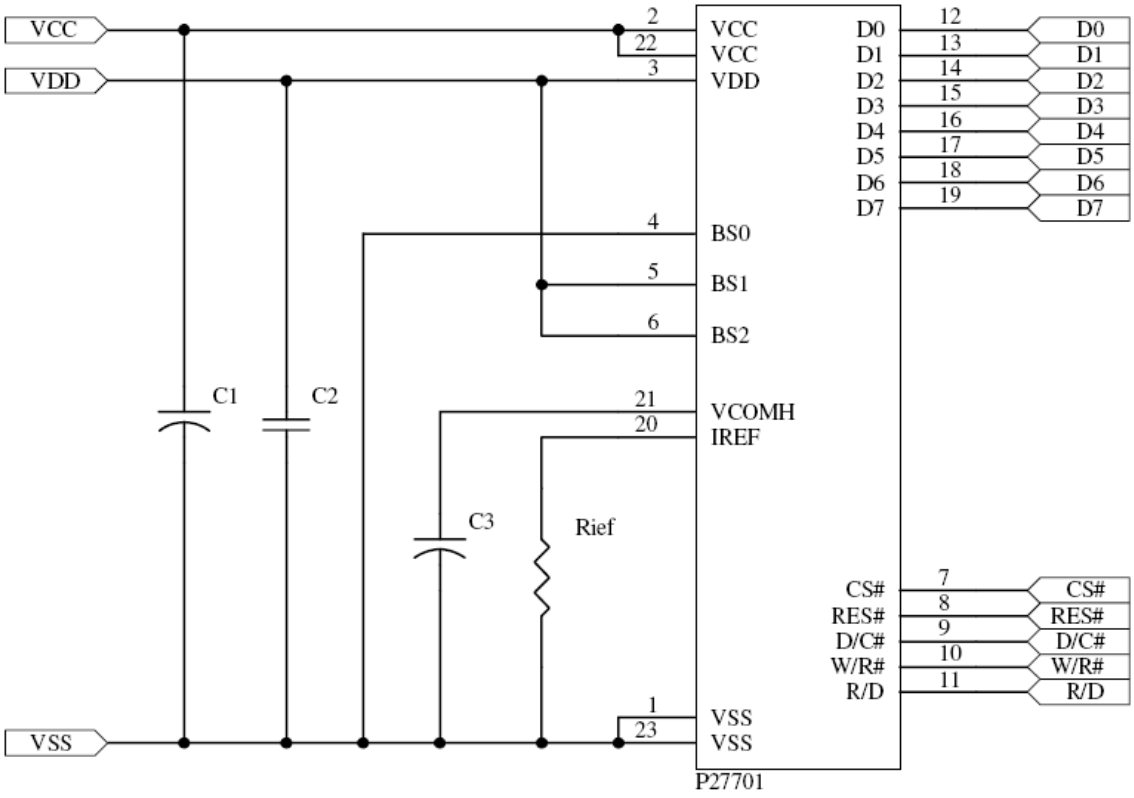
[1] V_{CC} should be disabled when it is OFF.

[2] Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

[3] The register values are reset after t_1.

[4] V_{DD} should not be Power OFF before V_{CC} Power OFF.

8.2 APPLICATION CIRCUIT



Component:

C1, C3: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

C2: 1uF/16V(0603)

R1: 1M ohm (0603) 1%

This circuit is for 8080 8bits interface

8.3 COMMAND TABLE

Refer to IC Spec.: SPD0301

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

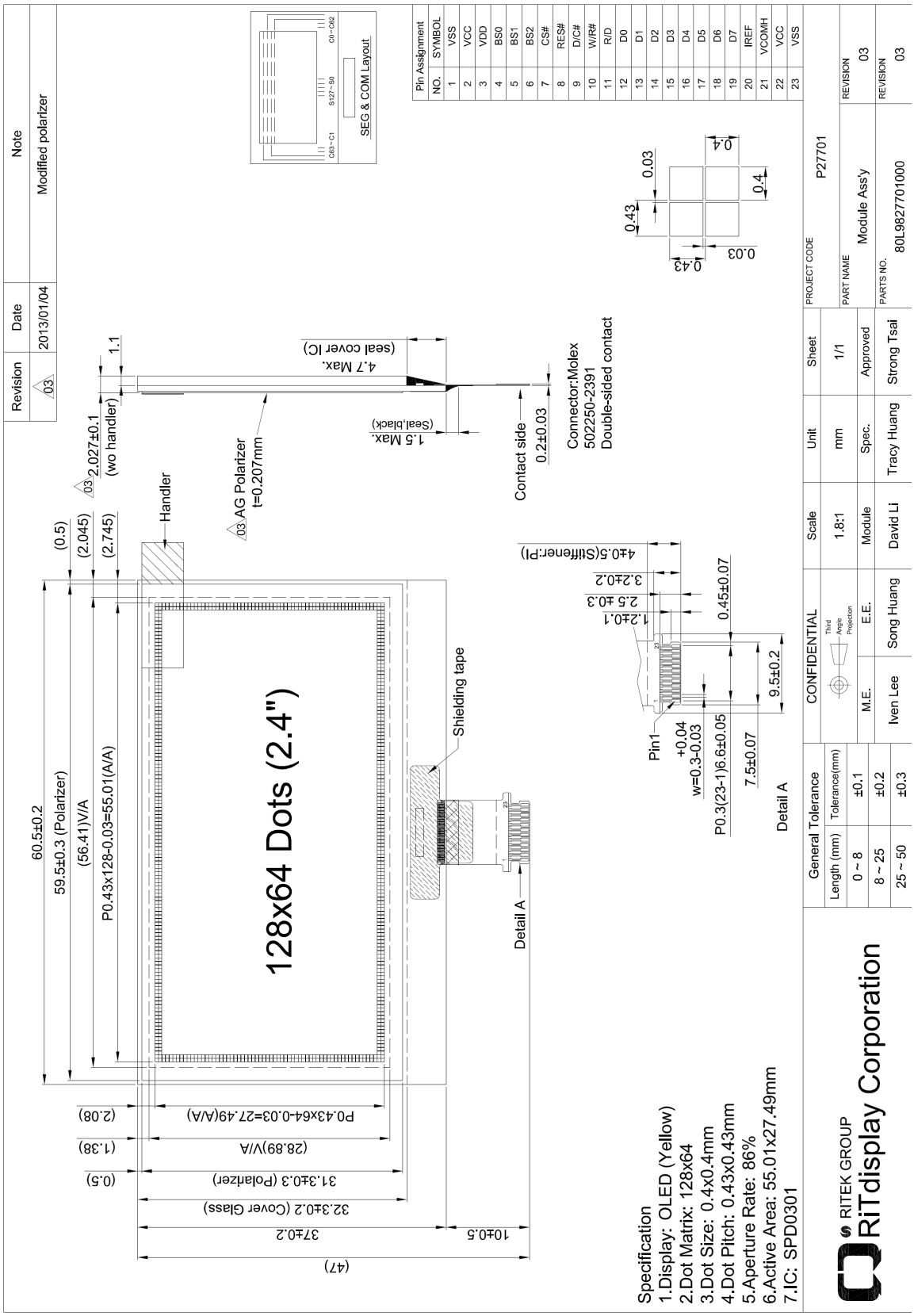
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION

TBD

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

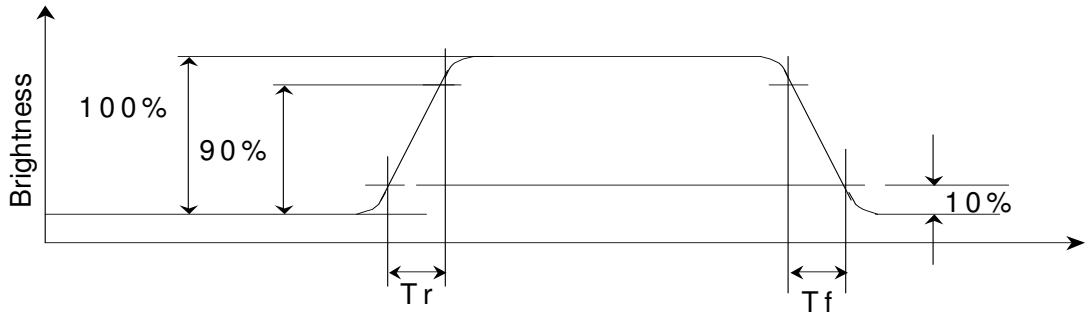


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

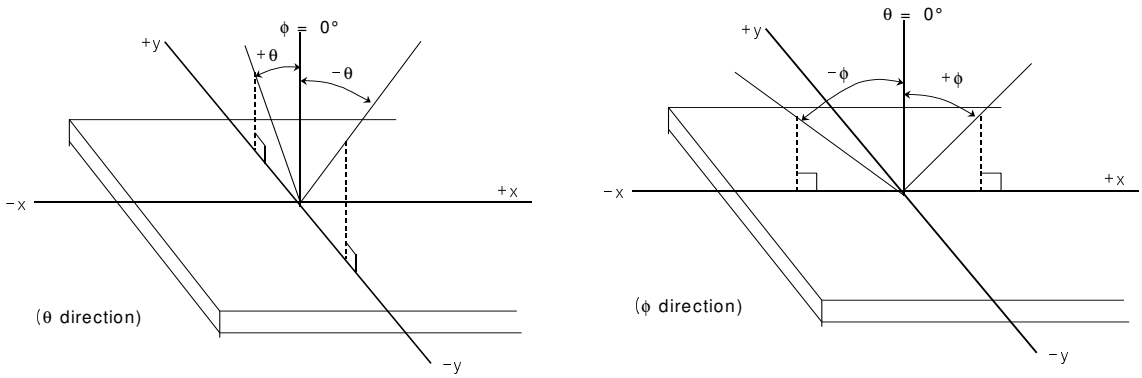
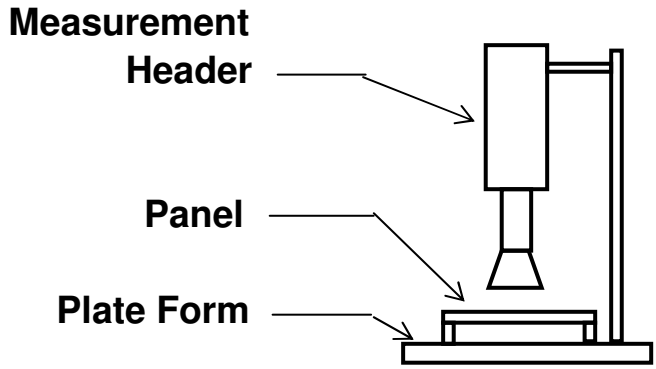


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

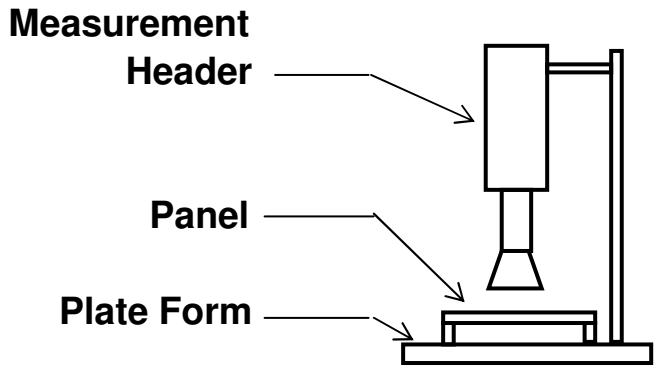
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA**

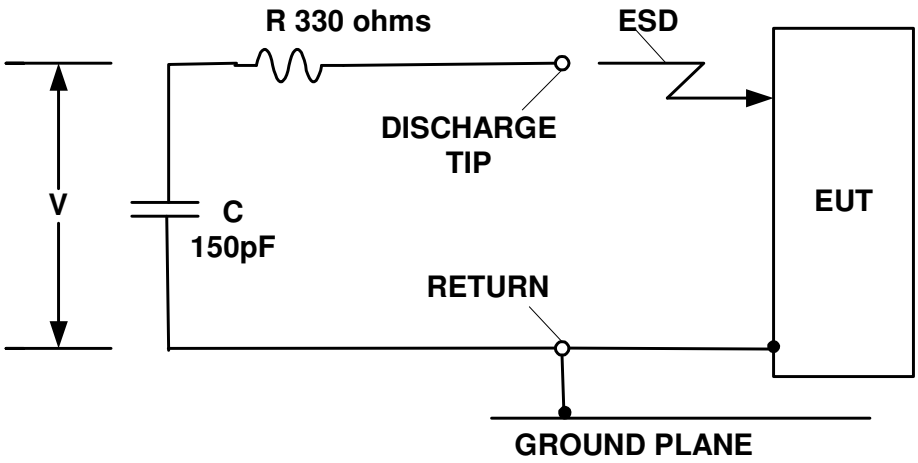
B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time
/**

C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.